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EXAMINER	
VIGUSHIN, JOHN B	
ART UNIT	PAPER NUMBER
2841	

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Please find below and/or attached an Office communication concerning this application or proceeding.

JK FF

Office Action Summary	Application No.	Applicant(s)
	10/661,616	FRALEY ET AL.
	Examiner	Art Unit
	John B. Vigushin	2841

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,9-11 and 15-24* is/are rejected.

7)☒ Claim(s) *8 and 12-14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *0903//15 Sept 2003*.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☒ Other: *See Continuation Sheet*.

Continuation of Attachment(s) 6). Other: Package Substrates: Internet article; 5 sheets.

DETAILED ACTION

Claim Objections

1. Claims 10 and 12 are objected to because of the following informalities in order to comply with 37 CFR 1.75(a):

In Claim 10, line 4: "layer" should be changed to --member--.

In Claim 12, the last line: "devices" should be changed to --chips--.

Appropriate correction is required.

Rejections Based On Prior Art

2. The following references were relied upon for the rejections hereinbelow:

Sylvester et al. (US 6,847,527 B2)
Katagiri et al. (US 6,841,881 B2)
Yoneda (US 6,781,221 B2)
Levardo et al. (US 6,753,613 B2)
Lo et al. (US 6,414,384 B1)
Kresge et al. (US 6,351,393 B1)*
Gallas (US 5,815,372)

Package Substrates, pp.1-5, article publ. 2002 by Sarang Shidore: found on Internet at:

http://www.coolingzone.com/Guest/News/NL_JAN_2002/Sarang/Jan_SS_2002.html

*Already made of record in Applicant's IDS filed September 15, 2003.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-3, 9 and 17-24 are rejected under 35 U.S.C. 102(e) as being anticipated by Katagiri et al. [Examiner's Note: *Package Substrates* is relied upon for indicating a structure not shown but inherent in Katagiri et al., in accordance with multiple reference § 102 rejections described in MPEP § 2131.01, part III].

As to Claims 1 and 16, Katagiri et al. discloses, in Fig. 37, a multichip electronic package comprising: an organic, laminate chip carrier 100 including a plurality of conducive planes spacedly positioned therein and separated by respective layers of dielectric material (col.5: 23-29 and col.6: 33-42), carrier 100 including a plurality of electrical contacts (wires 5 and pads 9) on a first surface thereof and a plurality of electrical conductors (wires 5 and pads 10) on a second surface thereof (col.5: 26-35 and col.6: 33-38), selected ones of electrical contacts 5 and 9 being electrically coupled to selected ones of the electrical conductors 5 and 10 (the interior wiring and via system that performs the coupling is not shown in Fig. 37, but is, inherently, part of the disclosed "built-up" multilayer structure of carrier 100, as shown in Fig. 37 and described on pp.4-5 of *Package Substrates* with an inner wiring and via arrangement that connects top and bottom surfaces, as shown in the accompanying Fig. 5 therein); and first and second semiconductor chips (first semiconductor chips 2A,B and second semiconductor chip 2C) positioned on the first surface of carrier 100 in a stacked

orientation, each chip electrically coupled to selected ones of contacts (wires 5 and pads 9).

As to Claim 2, Katagiri et al. further discloses selected ones of contacts 5 and 9 are electrically coupled to other selected ones of contacts 5 and 9 such that selected ones of chips 2A,B,C (chips 2A and 2C) are electrically coupled to one another (Figs. 8, 17 and 22; col.8: 22-24; col.10: 35-37 and 38-58).

As to Claim 3, Katagiri et al. further discloses first chip 2A is directly positioned on the first surface of carrier 100 and second chip 2C is positioned on first chip 2A (Fig. 37).

As to Claim 9, Katagiri et al. further discloses a quantity of encapsulant material 3 located on the first surface of carrier 100 and substantially covering both the first and second semiconductor chips (Fig. 37; col.1: 64-67 and col.10: 64-67).

As to Claim 17, Katagiri et al. further discloses electrically coupling first chip 2A is achieved using solder members 20 (Fig. 37; col.10: 31-37).

As to Claim 18, Katagiri et al. further discloses electrically coupling of second chip 2C is achieved using wirebond connections (Fig. 37; col.10: 47-53),

As to Claim 19, Katagiri et al. further discloses electrically coupling solder members 11 to selected ones of conductors 10, solder members 11 adapted to for electrically coupling the selected ones of conductors 10 to respective conductors on a circuitized substrate (Fig. 37; col.10: 67-col.11: 2; col.5: 30-37).

As to Claim 20, Katagiri discloses, in Fig. 37, a multichip electronic package assembly including: an organic, laminate chip carrier 100 including a plurality of

conducive planes spacedly positioned therein and separated by respective layers of dielectric material (col.5: 23-29 and col.6: 33-42), carrier 100 including a plurality of electrical contacts (wires 5 and pads 9) on a first surface thereof and a plurality of electrical conductors (wires 5 and pads 10) on a second surface thereof (col.5: 26-35 and col.6: 33-38), selected ones of electrical contacts 5 and 9 being electrically coupled to selected ones of the electrical conductors 5 and 10 (the interior wiring and via system that performs the coupling is not shown in Fig. 37, but is, inherently, part of the disclosed "built-up" multilayer structure of carrier 100, as shown in Fig. 37 and described on pp.4-5 of _Package Substrates_ with an inner wiring and via arrangement that connects top and bottom surfaces shown in the accompanying Fig. 5 therein); and first and second semiconductor chips (first semiconductor chips 2A,B and second semiconductor chip 2C) positioned on the first surface of carrier 100 in a stacked orientation, each chip electrically coupled to selected ones of contacts (wires 5 and pads 9); a circuitized substrate including electrically conductive members thereon and a plurality of electrically conductive elements 11 electrically connecting selected ones of conductors 10 on the carrier second surface to respective ones of the electrically conductive members on the circuitized substrate (not shown, but disclosed in col.5: 30-37).

As to Claim 21, Katagiri et al. further discloses the circuitized substrate is a printed circuit board (i.e., a wiring substrate *is* a printed circuit board; col.5: 35-37).

As to Claim 22, Katagiri et al. further discloses the plurality of electrically conductive elements 11 comprises solder members (Fig. 37; col.5: 35-37; col.10: 67-col.11: 2).

As to Claim 23, Katagiri et al. further discloses a first plurality of solder members 20 electrically coupling first semiconductor chip 2A to selected ones of electrical contacts 5 and 9 on the carrier first surface (Fig. 37; col.10: 31-37).

As to Claim 24, a plurality of wirebond connections 8 electrically coupling second chip 2C to other selected ones of the contacts 5 and 9 on the carrier first surface (Fig. 37; col.10: 50-53).

5. Claims 1-3, 9 and 17-19 are rejected under 35 U.S.C. 102(e) as being anticipated by Yoneda [Examiner's Note: *Package Substrates* is relied upon for indicating a structure not shown but inherent in Yoneda, in accordance with multiple reference § 102 rejections described in MPEP § 2131.01, part III].

As to Claims 1 and 16, Yoneda discloses, in Fig. 8, a multichip package comprising: an organic, laminate chip carrier 11 including a "built-up" substrate structure which is a type of organic laminate substrate that comprises a plurality of electrically conductive planes spacedly positioned therein and separated by respective layers of dielectric material (col.8: 41-50; built-up substrates defined on pp.4-5 of <u>Package Substrates</u>), carrier 11 including a plurality of electrical contacts 12 and 15 on a first surface thereof and a plurality of conductors (lands) on a second surface thereof (col.9: 64-66), selected ones of contacts 12, 15 being electrically coupled (by the inner wiring and via interconnects of the built-up substrate, not shown in Yoneda, but shown in Fig.

5 of *Package Substrates*) to selected ones of the conductors (lands) corresponding to solder bumps 40; first and second semiconductor chips 30 and 20, respectively, positioned on the first surface of carrier 11 in a stacked orientation, each chip 30 and 20 electrically coupled to selected ones of contacts 15 and 12, respectively.

As to Claim 2, Yoneda further discloses selected ones of contacts 12 are electrically coupled to other selected ones of contacts 15 such that stacked chips 30 and 20 are electrically coupled to one another (by way of wiring pattern 17 which is common to contacts 12 and 15; col.9: 20-41).

As to Claim 3, Yoneda further discloses first chip 30 is directly positioned on the first surface of carrier 11 and second chip 20 is positioned on first chip 30 (Fig. 8).

As to Claim 9, Yoneda further discloses a quantity of encapsulant material 36 located on the carrier first surface and substantially covering both chips 30 and 20 (Fig. 8; col.8: 1-10 and col.11: 18-20).

As to Claim 17, Yoneda further discloses electrically coupling of first chip 30 is achieved using a plurality of solder members 16 (col.9: 30-32 and 42-52; col.11: 31-37).

As to Claim 18, Yoneda further discloses electrically coupling second chip 20 is achieved using a plurality of wirebond connections 22 (Fig. 8; col.11: 14-17).

As to Claim 19, Yoneda further discloses including electrically coupling a plurality of solder members 40 to selected ones of the electrical conductors, the solder members 40 adapted for electrically coupling selected ones of the conductors to respective conductors on a circuitized substrate. [*Examiner's Note*: It has been held that the recitation that an element is "adapted to" perform a function is not a positive limitation

but only requires the ability to so perform. It does not constitute a limitation in any patentable sense. *In re Hutchison*, 69 USPQ 138].

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

8. Claims 4-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoneda in view of Levardo et al., Lo et al. and Katagiri et al.

A) As to Claim 4:

I. Yoneda discloses that the chips 30 and 20 may be, among other functional elements, an ASIC chip and/or a memory (col.5: 18-28) but does not specifically associate the particular function with one or the other of chips 30 and 20.

II. Levardo et al. discloses, in Fig. 12, first chip 102 and second chip 132, wire bonded and flip-chip bonded, respectively, as in Yoneda, and teaches that such chips may be, among other functional elements, an ASIC chip and/or a memory, and further teaches, specifically, that first chip 102 can be either wire bonded or flip-chip mounted ASIC (compare Figs. 7 and 12; col.3: 64-col.4: 1; and col.5: 51-57) but is silent as to the function of second wire-bonded chip 132.

III. Lo et al. teaches that ASICs, such as chip 409, are commonly used to support the functions of and drive the memory chips, such as chips 406 and 408 (col.4: 37-40 and 59-61) and Katagiri et al. teaches a stacked assembly of an ASIC chip 2C driving the memory chips 2A (Fig. 37; col.5: 19-22, col.9: 31-34, col.11: 10-12 and col.12: 20-23).

IV. Since Levardo et al., as well as Katagiri et al. teach a stacked chip assembly wherein the first chip is directly flip-chip mounted to the carrier and the second chip is positioned on the first chip and wire bonded to the carrier, and since Lo et al. and Katagiri et al. teach the use of ASICs as memory chip drivers in the same stacked package as the memory chips, then the use of a memory chip as the second wire-bonded chip 132 in Levardo et al., to be driven by the ASIC chip 102 below it, would have been readily recognized as an electronic application for the package of Levardo et al., and readily recognized in the same application in Yoneda as well, since Yoneda also has the stacked arrangement of a flip-chip mounted directly on the carrier and the wire-bonded chip positioned on the flip-chip, as in Levardo et al., and teaches that the chips may be an ASIC and/or memory, as in Levardo et al.

V. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use a memory chip for the wire-bonded chip in the stacked package of Yoneda as the chip being functionally supported and driven by a flip-chip mounted ASIC, as taught by Lo et al., wherein the ASIC is the first chip flip-chip directly onto the carrier and the memory is the second chip, positioned on the first chip and wire-bonded to the carrier, as taught by the structural disclosures of Levardo et al. and Katagiri et al.

B) As to Claim 5:

I. Modified Yoneda discloses first chip 30 is flip-chip coupled to selected ones of contacts 15 by a plurality of gold bumps (col.9: 7-13); not solder balls. Yoneda further discloses flexibility of chip type and arrangement in applications of the package disclosure (Fig. 8; col.12: 44-57).

II. Katagiri et al. further discloses at least two types of chips that can be flip-chip coupled to the carrier contacts; in a first embodiment, one type of chip 2A,B uses gold bumps 4 (Fig. 2; col.5: 1-6) and, in a second embodiment, another type of chip 2A uses solder balls 20 (Fig. 37; col.10: 5-7 and 31-37) for the purpose of adjusting the pitch of chip bonding pads to correspond to carrier contact pitch, pad arrangement and other wire routing requirements of the package (col.10: 5-14 and 31-37; and compare Figs. 2 and 37).

III. Since modified Yoneda and Katagiri et al. are both fabricating packages that include stacked chips coupled to a carrier, wherein one is flip-chip mounted and the other is wire bonded, then the use of solder balls instead of gold bumps for the purpose

of accommodating chip and carrier contact arrangements and other application requirements better suited for solder ball coupling than for gold-bump/solder-paste coupling technique, as taught by Katagiri et al., would have been readily recognized as an appropriate modification suitable for meeting the requirements of one any of various applications disclosed as admissible in the pertinent multichip package of Yoneda.

IV. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to further modify Yoneda with Katagiri et al. by replacing the gold bumps with solder bumps, as taught by Katagiri et al., in order to adjust the pitch of chip bonding pads to correspond to carrier contact pitch, pad arrangement and other wire routing requirements of an application of the package of Yoneda, as taught by Katagiri et al.

C) As to Claim 6, modified Yoneda further discloses second chip 20 is electrically coupled to selected ones of contacts 12 by wirebond connections 22 (Fig. 8; col.11: 14-17).

9. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yoneda in view of Levardo et al., Lo et al. and Katagiri et al., as applied to Claim 6, above, and further in view of Gallas.

I. Modified Yoneda does not include a heat-sinking member positioned substantially over the first and second semiconductor chips 30 and 20. Modified Yoneda further discloses protecting chips 30 and 20 and the other circuit elements with a humidity-resistant, electrically insulating resin encapsulant 36, such as an epoxy resin, for example (Fig. 8; col.8: 1-10 and col.11: 18-20).

II. Gallas discloses, in Fig. 5, the same stacked chip arrangement disclosed in modified Yoneda (chip 54 is flip-chip mounted and chip 64 is wire bonded to carrier 56; col.3: 31-37 and col.4: 10-16) including encapsulant 58 (col.4: 38-42), but further discloses that encapsulant 58 not only protects the circuit elements but is made of a thermally conductive material which further enables the practical use of a heat sinking member attached to the encapsulant (i.e., positioned over the first and second chips) for the purpose of dissipating the heat generated by the stacked chips (col.4: 43-50).

III. Since Yoneda and Gallas are both practitioners in the fabrication of electronic packages including stacked semiconductor chips, the problem of heat generated by the stacked assembly during operation solved by a thermally conductive encapsulant coupled with a heat sink member, as taught by Gallas, would have been readily recognized as a vital modification to the stacked chip assembly of Yoneda for the same purpose as in the stacked chip assembly of Gallas.

IV. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to further modify the stacked chip assembly, with encapsulant, of Yoneda with the thermally conductive encapsulant and the heat-sinking member attached thereto of Gallas, whereby, the heat-sinking member is positioned substantially over the first and second stacked chips in Yoneda, as taught by Gallas, in order to dissipate the heat generated by the stacked chip assembly of Yoneda during operation, thus ensuring package reliability, as taught by Gallas.

10. Claims 10 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoneda in view of Kresge et al.

A) As to Claim 10:

I. Yoneda further discloses a plurality of solder elements 16 electrically coupling the gold bumps 32 of first semiconductor (col.8: 53-55) chip 30 to selected ones of contacts 15 on the organic (col.8: 41-50) carrier first surface (col.9: 11-13, 30-32 and 42-52; col.11: 31-37).

II. Yoneda does not disclose a thermally conductive member in carrier 11, the thermally conductive member having a selected thickness and coefficient of thermal expansion (CTE) to substantially prevent failure of electrical coupling formed by the solder elements 16 on selected ones of contacts 15 due to CTE mismatch between first chip 30 of the stacked chip assembly and organic carrier 11.

III. Kresge et al. discloses an organic carrier 18 having a semiconductor chip 12 mounted thereon, the chip 12 and electrically coupled to organic carrier 18, chip 12 having C4 (i.e., high melting point) solder members 16 coupled to contacts 40 of carrier 18 through electrical couplings formed by solder elements 47 (low temperature or eutectic solder). Kresge et al. further teaches a thermally conductive layer 22 in carrier 18 for the dual purposes of preventing package malfunction through overheating during operation and having a selected thickness and CTE to substantially prevent failure of the electrical couplings formed by solder elements 47 on selected ones of carrier contacts 40 due to CTE mismatch between semiconductor chip 12 and organic carrier 18 (col.5: 40-col.6: 12).

IV. Although Yoneda does not address in the disclosure the issue of thermal dissipation of heat during package operation and CTE mismatch between

semiconductor material chip and organic material carrier and the resultant stress forces on the solder element electrical couplings, that are old and well-known in the packaging art, nevertheless both Yoneda and Kresge et al. are in the packaging art wherein a chip carrier is mounted to a system board for operation in an electronic system where heat during operation increases the temperature of the package and inherently results in thermal expansion of chips and carrier at different rates represented by the different respective chip and carrier CTEs. Accordingly, the problem of dissipating heat generated by the chips on the carrier, thereby preventing overheating of the package, and the problem of CTE mismatch between semiconductor chip and organic board would have been problems inherently encountered in the pertinent art of Yoneda, and the solution to both of those problems, provided by the thermally conductive member taught in Kresge et al., would have been readily recognized as a solution to the overheating and thermal expansion mismatch problems ineluctably encountered in the similar chip carrier package disclosed in the pertinent art of Yoneda.

V. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the carrier of Yoneda with the thermal conductive member of Kresge et al., wherein the thermal conductive member thickness and material composition are selected to optimize thermal dissipation and reduction of chip/carrier CTE mismatch in order to prevent the carrier package from overheating and to prevent failure of the chip/carrier couplings formed by the solder elements, thereby greatly enhancing package performance reliability in Yoneda, as taught by Kresge et al.

B) As to Claim 11, modified Yoneda further discloses the thermally conductive member is comprised of a first layer of copper, a second layer of iron alloy and third layer of copper for achieving optimal thermal conductivity and CTE mismatch reduction (Kresge et al., col.5: 48-54).

11. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yoneda in view of Sylvester et al.

I. Yoneda discloses an organic, laminate ("built-up") carrier 11 (col.8: 41-50) having semiconductor chips 30 and 20 mounted thereon but does not teach that carrier 11 includes an internal capacitor within the carrier.

II. Sylvester et al. discloses the use of capacitors in semiconductor chip carriers as decoupling capacitors for achieving a low impedance between chip and power/ground planes or lines in order to ensure optimal decoupling of power/ground plane or line noise, and further discloses an organic, laminate carrier (see Figs. 4 and 5, for example, and col.1: 19-25; the carrier being formed of organic materials, as indicated in col.7: 60-col.8: 5) comprising an internal core capacitor structure 26 (col.7: 46-52 for Fig. 4 and col.9: 20-27 for Fig. 5) as an alternative to the use of discrete chip capacitors. Replacing prior art chip capacitors with internal capacitors--i.e., capacitors built into the laminate structure of the carrier--solves the problem of parasitic inductances that typically occur in chip capacitors at the high operational frequencies used in current electronic applications (col.1: 38-50 and col.2: 1-15), thereby optimizing the impedance controlling function of the capacitors.

III. The carrier of Yoneda inherently has at least one power plane/line and ground (i.e., return) plane/line which would benefit from the impedance control afforded by use of a capacitor as a decoupling capacitor, as taught by Sylvester et al., and moreover, an *internal* decoupling capacitor to optimize the impedance control performance of the decoupling capacitor for ensuring a low impedance between chip and power and ground distribution lines in Yoneda, hence excellent noise suppression, as taught by Sylvester et al.

IV. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the laminate carrier of Yoneda by including an internal capacitor therein in order to optimally perform the impedance control function of a decoupling capacitor for ensuring a low impedance between the stacked chips mounted on the carrier and the power/ground distribution lines and optimal noise decoupling in the carrier of Yoneda, thereby, as taught by Sylvester et al.

12. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Katagiri et al.

I. Katagiri et al. discloses an organic, laminate ("built-up") carrier 100 (Fig. 37) having semiconductor chips 2A, 2C mounted thereon and further teaches a noise decoupling chip capacitor mounted *on* the carrier (col.11: 33-38) but does not teach that carrier 100 includes an internal capacitor within the carrier.

II. Sylvester et al. discloses the use of capacitors in semiconductor chip carriers as decoupling capacitors for achieving a low impedance between chip and power/ground planes or lines in order to ensure optimal decoupling of power/ground

plane or line noise, and further discloses an organic, laminate carrier (see Figs. 4 and 5, for example, and col.1: 19-25; the carrier being formed of organic materials, as indicated in col.7: 60-col.8: 5) comprising an internal core capacitor structure 26 (col.7: 46-52 for Fig. 4 and col.9: 20-27 for Fig. 5) as an alternative to the use of discrete chip capacitors. Replacing prior art chip capacitors with internal capacitors--i.e., capacitors built into the laminate structure of the carrier--solves the problem of parasitic inductances that typically occur in chip capacitors at the high operational frequencies used in current electronic applications (col.1: 38-50 and col.2: 1-15), thereby optimizing the impedance controlling function of the capacitors.

III. Since Katagiri et al. and Sylvester et al. both teach capacitors that decouple power/ground line noise and Sylvester et al. further teaches the improved low impedance between chip and power/ground planes or lines achieved by use of an internal decoupling capacitor instead of a surface mounted discrete chip capacitor, then the enhanced noise decoupling performance of the internal capacitor of Sylvester et al. would have been readily recognized for the same enhanced noise suppression in the multichip package of Katagiri et al.

IV. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the laminate carrier of Katagiri et al. by replacing the decoupling chip capacitor with an internal capacitor within the carrier, as taught by Sylvester et al., in order to optimally perform the impedance control function of a decoupling capacitor for ensuring a low impedance between the stacked chips mounted

on the carrier and the power/ground distribution lines and optimal noise decoupling in the carrier of Katagiri et al., thereby, as taught by Sylvester et al.

13. Claims 20-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoneda in view of Katagiri et al.

A) As to Claim 20:

I. Yoneda discloses, in Fig. 8, a multichip package comprising: an organic, laminate chip carrier 11 including a "built-up" substrate structure which is a type of organic laminate substrate that comprises a plurality of electrically conductive planes spacedly positioned therein and separated by respective layers of dielectric material (col.8: 41-50; see also built-up substrates described on pp.4-5 and Fig. 5 of _Package Substrates_), carrier 11 including a plurality of electrical contacts 12 and 15 on a first surface thereof and a plurality of conductors (lands) on a second surface thereof (col.9: 64-66), selected ones of contacts 12, 15 being electrically coupled (by the inner wiring and via interconnects of the built-up substrate, not shown in Yoneda, but is, inherently, a part of the multilayer "built-up" structure of the carrier of Yoneda, as described and shown on pp.4-5 and Fig. 5 of _Package Substrates_) to selected ones of the conductors (lands) corresponding to solder bumps 40; first and second semiconductor chips 30 and 20, respectively, positioned on the first surface of carrier 11 in a stacked orientation, each chip 30 and 20 electrically coupled to selected ones of contacts 15 and 12, respectively; Yoneda discloses electrically conductive elements 40 connecting selected ones of the electrical conductors on the carrier second surface to respective ones of electrically conductive members on an external device not shown. Yoneda does not

disclose that the device is a circuitized substrate including electrically conductive members thereon to which the conductive elements 40 are connected.

II. Katagiri et al. discloses a circuitized substrate including electrically conductive members thereon and a plurality of electrically conductive elements 11 electrically connecting selected ones of conductors 10 on the carrier second surface to respective ones of the electrically conductive members on the circuitized substrate (not shown, but disclosed in col.5: 30-37).

III. Since both Yoneda and Katagiri et al. both teach the same type of stacked chip package, then connecting the conductors on the carrier second surface to the conductive members of a circuitized substrate as the external device for establishing an electrical connection as part of an electronic system, as taught by Katagiri et al., would have been readily recognized in the pertinent packaging art of Yoneda.

IV. Therefore, it would have been obvious to provide a circuitized substrate including electrically conductive members thereon for the plurality of electrically conductive elements to electrically connect selected ones of conductors on the carrier second surface to respective ones of the electrically conductive members on the circuitized substrate as an application of the carrier package of Yoneda to an electronic system application, as taught by Katagiri et al.

B) As to Claim 21, the circuitized substrate of Yoneda, as modified by Katagiri et al. (col.5: 30-37) *is* a printed circuit board.

C) As to Claim 22, modified Yoneda further discloses conductive elements 40 are solder balls (Fig. 8; col.9: 20-24).

D) As to Claim 23, modified Yoneda further discloses a first plurality of solder members 16 electrically coupling first chip 30 to selected ones of contacts 15 on the carrier first surface (col.9: 30-32 and 42-52; col.11: 31-37).

E) As to Claim 24, modified Yoneda further discloses second chip 20 is electrically coupled to selected ones of contacts 12 by wirebond connections 22 (Fig. 8; col.11: 14-17).

Allowable Subject Matter

14. Claims 8 and 12-14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

15. The following is a statement of reasons for the indication of allowable subject matter:

As to Claim 8, patentability resides in *the heat-sinking member being positioned on the stiffener member*, in combination with the other limitations of the claim.

As to Claims 12-14, patentability resides in *at least one conductive plane of a first multilayered portion includes signal lines capable of having signals pass therealong at a first frequency and a second conductive signal plane of a second multilayered portion includes signal lines capable of having signals pass therealong at a higher frequency than the first frequency*, in combination with the other limitations of the broadest claim, Claim 12.

16. As allowable subject matter has been indicated, applicant's reply must either comply with all formal requirements or specifically traverse each requirement not complied with. See 37 CFR 1.111(b) and MPEP § 707.07(a).

Conclusion

17. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

McCormick (US 6,369,448 B1) discloses the use of heat sinks and/or stiffeners in conjunction with package comprising the disclosed stacked flip-chip assembly on a carrier, wherein the heat sink and/or stiffener may attached to the backside of the top chip (col.3: 53-57; col.4: 35-41; col.6: 61-65; col.7: 12-15).

18. Any inquiry concerning this communication or earlier communications from the examiner should be directed to John B. Vigushin whose telephone number is 571-272-1936. The examiner can normally be reached on 8:30AM-5:00PM Mo-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John B. Vigushin
Primary Examiner
Art Unit 2841

jbv
May 27, 2005